Beamtest results of the CBM-TRD feature extraction using SPADIC v1.0*

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The feature extraction is a data processing stage of the proposed data acquisition chain (DAQ) for the CBM/TRD experiment aiming to deliver event-filtered and bandwidth-reduced data to the First Level Event Selection (FLES). The feature extraction processing stage will be implemented at the Data Processing Board (DPB) located in the TRD-DAQ. A data rate of about 1TB/s and a high event rate of approximately 10 MHz is expected for the final experiment [1].

In October and November 2012 a common CBM subsystems (RICH/TRD/TOF) beam test was performed at the CERN Proton Synchrotron (PS) T9 accelerator beamline [2]. A full size (59×59 cm^2) TRD detector prototype from Münster [3], with an amplification/drift region of 7.0/5.0 mm was used for this experimentation. The readout and signal processing of the TRD module was performed by the Self-triggered Pulse Amplification and Digitization asIC (SPADIC) version 1.0 [4]. The SPADIC chip reads out 32 channels in self-triggered mode and, compared to the previous SPADIC v0.3 chip, it implements new features which are of importance for the feature extraction (e.g. neighbor channel-trigger readout).

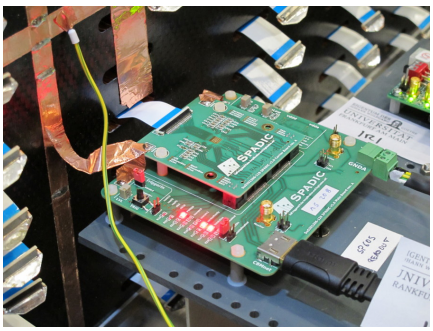

Figure 1: Full size TRD prototype and SPADIC v1.0 PCB. Experimental setup in the CERN PS/T9 in 2012.

In order to perform further developments for the feature extraction stage, obtaining real data samples from TRD full size prototypes by means of the new SPADIC v1.0 chip, was one of the main purposes during the beam test in the CERN PS T9. The experimental data acquisition setup was composed of the SPADIC v1.0 connected by a HDMI cable to a Readout Controller (ROC). The latter was interfaced with an optical connection to an Active Buffer Board (ABB) in a data acquisition computer. The communication protocol used was CBMnet 2.0 [5]. An effective area of 16 channels were read out in self-triggered mode, however, a total area of 8 channels were read out using the neighbor channel-trigger feature. A set of recorded data was acquired during the beam test, however, this data set lacks of synchronization to any other subsystem detector.

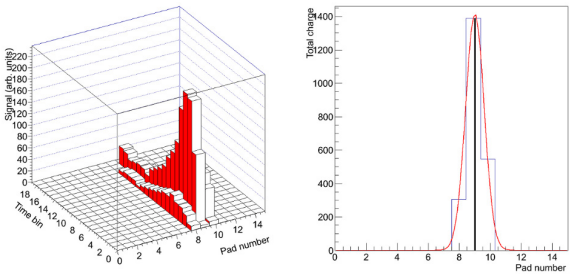

Figure 2: Left plot, reconstructed TRD cluster for a single particle. Right plot, hit position approximation by a fit on total charge deposition. The central fit line indicates the reconstructed hit position.

An online cluster reconstruction is currently being designed using beam test data. Even if it is not possible to reconstruct the whole physical event, it helps to simulate specific high particle rates scenarios in order to develop a DPB feature extraction module. As shown in Figure 2, a 3 pad cluster and its approximated position reconstruction were obtained using a clusterizer algorithm that is easily parallelizable. Furthermore, the firmware migration of the actual feature extraction processing board (Xilinx SP605 FPGA) into the new SysCore v3 [6] will be one of the main tasks in 2013.

* Work supported by BMBF (06HD9123I, 06FY7090)

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